

## AMENDMENTS TO CLAIMS

### Listing of Claims

*sub E1*  
C1  
52. (Currently amended) A semiconductor component comprising:

a substrate comprising a plurality of tested semiconductor components including a plurality of good components and at least one defective component; ~~and~~

a plurality of conductors on the substrate configured to provide electrical paths to the good components while electrically isolating the at least one defective component; and

a plurality of terminal contacts on the conductors.

*sub E1*  
53. (Previously amended) The component of claim 52 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or semiconductor packages.

*C2 sub E1*  
54. (Currently amended) The component of claim 52 wherein the conductors comprise a metal laser patterned redistribution layer.

*sub E1*  
55. (Withdrawn) The component of claim 52 wherein the conductors are configured to electrically connect multiple components in a cluster that excludes the at least one defective component.

*sub E1*  
C3  
cont  
56. (Currently amended) A semiconductor component comprising:

a substrate comprising a plurality of tested components, each component comprising a plurality of component contacts;

the components including a plurality of good components and a defective component; ~~and~~

*C3 would*  
a plurality of ~~laser patterned~~ conductors on the substrate configured to provide electrical paths ~~between~~ for the component contacts on the good components and to electrically isolate ~~7~~ the component contacts on the defective component; and

a plurality of terminal contacts on the good components in electrical communication with the conductors.

*sub E1*  
57. (Previously amended) The component of claim 56 wherein the conductors comprise a metal redistribution layer.

58. (Withdrawn) The component of claim 56 wherein the conductors are configured to electrically connect a plurality of good components in a cluster.

59. (Currently amended) The component of claim 56 wherein the substrate comprises a semiconductor wafer, and the components comprise semiconductor dice or semiconductor packages.

60. (Withdrawn) A semiconductor component comprising:

a semiconductor die comprising a plurality of integrated circuits and a plurality of component contacts in electrical communication with the integrated circuits;

a plurality of conductors on the die in electrical communication with the component contacts; and

a plurality of terminal contacts on the die in electrical communication with the conductors;

at least some of the conductors configured to interconnect or electrically isolate selected component

contacts or selected terminal contacts to repair defects on the die.

61. (Withdrawn) The component of claim 60 wherein the terminal contacts comprise a ball grid array.

62. (Withdrawn) The component of claim 60 wherein the conductors comprise a laser patterned redistribution layer.

63. (Withdrawn) A test board for testing semiconductor components on a substrate comprising:

a plurality of test sites on the test board configured to electrically engage the components on the substrate;

the test sites comprising a plurality of conductors configured to provide electrical paths to the components and to electrically isolate at least one component on the substrate.

64. (Withdrawn) The test board of claim 63 wherein the conductors comprise a laser patterned metal layer.

65. (Withdrawn) The test board of claim 63 wherein the test board is configured to perform a burn-in test.

66. (Withdrawn) The test board of claim 63 wherein the substrate comprises a wafer, and the components comprise dice or packages.

67. (Canceled) A system for fabricating semiconductor components comprising:

a substrate comprising a plurality of semiconductor components;

a test circuitry configured to test the semiconductor components; and

a laser scanner configured to pattern a metal layer deposited on the components and the substrate using data obtained by the test circuitry.

68. (Canceled) The system of claim 67 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or packages.

69. (Canceled) The system of claim 67 further comprising a test board configured to electrically engage the components for performing a burn-in test.

70. (Withdrawn) A semiconductor component comprising:

a semiconductor die comprising a plurality of integrated circuits including at least one defective integrated circuit;

a plurality of terminal contacts on the die; and

a redistribution layer on the die comprising a plurality of laser patterned conductors configured to electrically connect the terminal contacts to the integrated circuits and to electrically isolate the terminal contacts from the at least one defective integrated circuits.

71. (Withdrawn) The component of claim 60 wherein the terminal contacts comprise balls or bumps in a grid array.

*Sub E1  
Concl 1*

72. (Withdrawn) The component of claim 60 further comprising a plurality of bond pads on the die in electrical communication with the integrated circuits and the conductors.

73. (Withdrawn) The component of claim 60 wherein the redistribution layer comprises a metal.

74. (Withdrawn) The component of claim 60 wherein the conductors are separated by etched openings.

75. (Withdrawn) The component of claim 60 further comprising a protective layer on the conductors having a plurality of openings for the terminal contacts.

76. (Withdrawn) The component of claim 60 wherein the conductors comprise a deposited metal.

77. (Withdrawn) The component of claim 60 wherein the conductors are configured to repair the at least one defective integrated circuits.